



## Final deliverable

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Abstract **This report summarizes the work done on Tools for model management of the WP5**

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Keyword List VHDL-AMS, translator, compiler.

## SUMMARY

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### 1.INTRODUCTION

As the user needs to write envelope and accuracy boundereis for wiring and harness elements model view or modify existing models, he will use a textual modelling language to describe components behaviour. This language will be checked and compiled to be understandable by the harness behaviour simulator.

The modelling language chosen is VHDL-AMS for this application and a compiler has been developed to check the model written in this language and to generate a Delphi model, where Delphi is a language understandable by the simulator.

### 2.VHDL-AMS

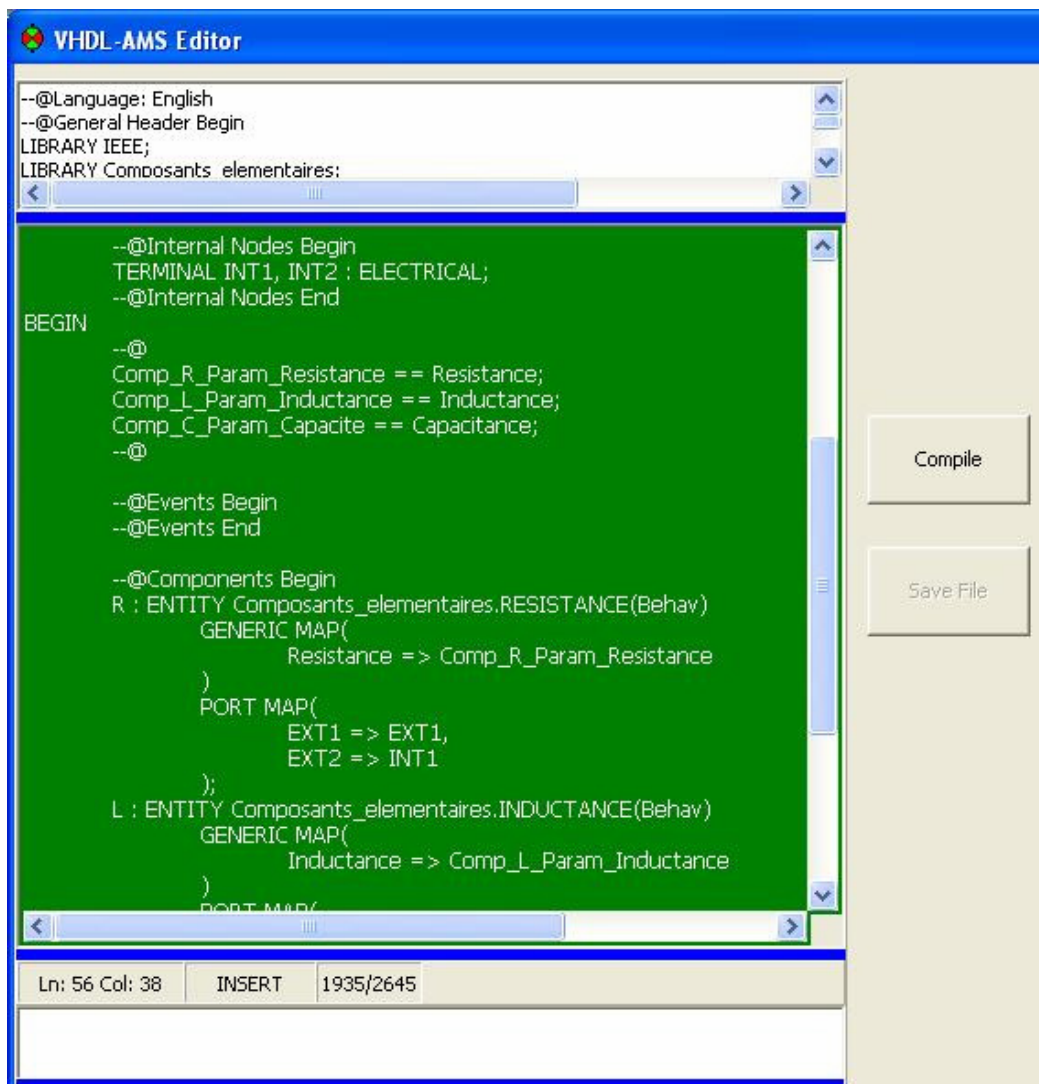
VHDL-AMS is the Analog and Mixed-Signal extension to the Very High Speed Integrated Circuit Hardware (VHDL). VHDL-AMS provides behavioral modeling capability for discrete, continuous and mixed systems. The continuous systems are described using Differential Algebraic Equations (DAEs). VHDL-AMS also provides mixed-discipline modeling, so different domains such as electrical and thermal can be described and simulated in a single entity. The main features of this language are Mixed-signal modeling, Behaviora modeling, Signal Flow Semantics, Mixed-tecnology modeling and Transparency.

### 3.VHDL-AMS TRANSLATOR

After choosing the VHDL-AMS language, a first version of a translator has been developed by CEIT to obtain VHDL-AMS files from the data structure of ALGO'TECH simulator and from ".ini" files. The final target is to complete a model library containing VHDL-AMS files describing all the electric components detailed in chapter ATA-24. Complex models will be developed from the simple ones according to a structural architecture of VHDL-AMS files.

#### 4.VHDL-AMS EDITOR

To allow the user to edit the VHDL-AMS file generated by the translator a VHDL-AMS Editor has been developed. The Figure 1 shows the main window of the Editor.



**Figure1. VHDL-AMS Editor**

The code of the VHDL-AMS file generated is shown on the first window of the screen. On the second one, part of the VHDL-AMS file that the user can edit is shown.

The user is allowed to edit the part of the VHDL-AMS code corresponding to the Architecture part.



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### 5.VHDL-AMS COMPILER

A VHDL-AMS Compiler has been designed and developed to check the VHDL-AMS code of the model. After the research of the existing tools needed to develop a compiler, it decided to develop it in the same programme language the ALGO'TECH simulator have been developed. The aim of developing a compiler is to integrate it in the simulator. The fact that the code is written in the same programme language simplifies the integration.

To make this compiler it was necessary to develop and design a lexical analyzer, syntax analyzer and semantic analyzer.

- Lexical Analyzer checks the source code of the input file to find any lexical error. For example: when the 'si' is written instead of 'is'.
- Syntax Analyzer checks the input file code to find any syntax error. For example: when the if conditional sentence has not been written incorrectly.
- Semantic Analyzer checks the input file code to find any semantic error. For example: when an undeclared variable is used in the code source.

### 6.VHDL-AMS EDITOR INTEGRATED IN THE ALGO'TECH SIMULATOR

After developing the VHDL-AMS Editor, on completion of the three analyzers described previously, it was found necessary to make some changes in the both VHDL-AMS Editor and Algo'tech Simulator. Finally the Simulator supplies the models in vhdL-ams code to the VHDL\_AMS Editor, then from the VHDL-AMS editor the code can be edited and compiled by the user.

### 7.DELPHI MODEL

When the code is written correctly, is necessary to translate it in Delphi language in order to obtain the model in the same language program that the simulator is developed. During compilation, the information of the model saved is written in Delphi code to obtain the same model in the Delphi language.

### 8.CONCLUSION

As the ALGO'TECH Simulator works with models developed in its programming language and the aim of the task 5.2 is to allow the user to edit the model, a translator have been developed to translate the model in the simulator's language to VHDL-AMS language and the translation is shown in an Editor. In order to correct the changes made by the user, the lexical, syntactic and semantic analyzer have been developed. Finally, when the model written in VHDL-AMS language is correct, the model saved in the simulator is a model written in Delphi language. Delphi is a programming language understandable by the Simulator.

This tools developed allow the user to manage the models of the ALGO'TECH Simulator.